Specification

Please replace the paragraphs beginning on page 9, line 12 with the following:

In addition, the number of times in writing the data to the variables loaded onto the evaluated bus represents a number of times in effecting data transfer on the evaluated bus, namely bus traffic. Because the processing rate requested by the main function is already known, it is possible to calculate the bus traffic for the processing rate and effect performance evaluation in accordance with the following equation (1).

(Bus traffic for the processing rate)

= (number of times in effecting data transfer) / (processing rate) ... (1)

To change the bus interconnecting the hardware and software in response to the bus traffic being calculated for the processing rate, the sources used in the algorithm design are modified so that the simulation ~~platform~~ program is to be structured again.

Please replace the paragraph beginning on page 9, line 22 with the following:

FIG. 3 shows an example of the 'restructured' simulation ~~platform~~ program. With reference to the restructured simulation program shown in FIG. 3, the variable b is regarded as one that is not to be loaded onto the evaluated bus because of result of the performance evaluation of the bus. That is, the restructured simulation program has only two variables a, b that are being loaded onto the evaluated bus. Since the variable b is not loaded onto the bus, the evaluation function BUS0() is not embedded subsequent to the variable b to which data is written. In contrast, the evaluation function BUS0() is certainly embedded subsequent to the variables a, c to which data are written respectively. Thus, the evaluation function BUS0() is certainly executed just after the variables a, c to which the data are written respectively.